



AK7738VQ
AKM Semiconductor

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AK7738

Multi DSP with 5ch ADC + 4ch DAC + 8ch SRC

1. General Description

The AK7738 is a highly integrated digital signal processor, including a 24-bit stereo ADC with MIC gain amplifiers, a 24-bit stereo ADC with input selector, a monaural ADC, two 32-bit stereo DACs, 4 stereo sampling rate convertors supporting the sampling frequency up to 192kHz, two DSPs and a Sub DSP for Audio/HF process. Each two DSPs and a Sub DSP has 2560step/fs (when fs=48kHz) parallel processing power. The AK7738 is capable of processing sound and voice such as for hands-free function simultaneously because two DSPs are able to work on different but synchronized sampling frequencies. As the AK7738 is a RAM based DSP, it is freely programmable for user requirements, such as acoustic effects and proprietary high performance hands-free function. The AK7738 is available in a 64-pin LQFP package.

2. Features

- **DSP1/DSP2: (Memory areas are shared by DSP1 and DSP2)**
 - **Word length:** 28-bit (Simple floating point supported)
 - **Instruction cycle:** 8.1ns (2560fs at fs=48kHz)
 - **Multiplier:** 24 x 24 → 48-bit (Double precision arithmetic available)
 - **Divider:** 24 / 24 → 24-bit (Floating point normalization function)
 - **ALU:** 52-bit arithmetic operation (with 4bits overflow margin)
 - **Program RAM:** 8192 word x 36-bit
 - **Coefficient RAM:** 6144 word x 24-bit
 - **Data RAM:** 6144 word x 28-bit
 - **Delay RAM:** 20480 word x 28-bit
 - **JX pins (Interrupt)**
 - **Clock Mode Selector for DSP1, DSP2**
 - **Independent Power Management Function for DSP1, DSP2**
- **Sub DSP**
 - **Word length:** 28-bit (Simple floating point supported)
 - **Instruction cycle:** 8.1ns (2560fs at fs=48kHz)
 - **Multiplier:** 24 x 24 → 48-bit (Double precision arithmetic available)
 - **Divider:** 24 / 24 → 24-bit (Floating point normalization function)
 - **ALU:** 52-bit arithmetic operation (with 4bits overflow margin)
 - **Program RAM:** 1024 word x 36-bit
 - **Coefficient RAM:** 2048 word x 24-bit
 - **Data RAM:** 4096 word x 28-bit
- **ADC1: 24-bit Stereo ADC with MIC Gain Amplifiers**
 - **Sampling Frequency:** fs=8kHz to 192kHz
 - **Channel Independent Analog Gain Amplifiers**
(0 to 18dB(2dB Step), 18 to 36dB(3dB step))
 - **Differential Input or Single-ended Input**
 - **ADC Characteristics** S/N: 102dB (fs=48kHz, Differential Input, MIC Gain=0dB,)
 - **Channel Independent Digital Volume Control** (+24 to -103dB, 0.5dB Step, Mute)
 - **Analog DRC (Dynamic Range Control)**
 - **Digital HPF for DC Offset Cancelling**
 - **Low Noise MIC Power Output: 2ch**
 - **4 types of Digital Filter for Sound Color Selection**

- **ADC2: 24-bit Stereo ADC with Input Selector**
 - Sampling Frequency: $f_s=8\text{kHz}$ to 192kHz
 - Analog Input Selector: Differential Input x1 or Single-ended Input x2, Semi-Differential Input x1
 - ADC Characteristics S/N: 102dB ($f_s=48\text{kHz}$, Differential Input)
 - Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)
 - Digital HPF for DC Offset Cancelling
 - 4 types of Digital Filter for Sound Color Selection
- **ADCM: 24-bit Monaural ADC**
 - Sampling Frequency: $f_s=8\text{kHz}$ to 192kHz
 - Differential Input or Single-ended Input
 - ADC Characteristics S/N: 102dB ($f_s=48\text{kHz}$, Differential Input)
 - Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)
 - Digital HPF for DC Offset Cancelling
 - 4 types of Digital Filter for Sound Color Selection
- **DAC: Advanced 32-bit DAC**
 - 2ch x2
 - Sampling Frequency: $f_s=8\text{kHz}$ to 192kHz
 - Single-ended Output
 - DAC Characteristics S/N: 108dB ($f_s=48\text{kHz}$)
 - Channel Independent Digital Volume Control (+12 to -115dB, 0.5dB Step, Mute)
 - 4 types of Digital Filter for Sound Color Selection
- **SRC:**
 - 2ch x4
 - FSI = 8kHz to 192kHz , FSO = 8kHz to 192kHz (FSO/FSI = 0.167 to 6.0)
- **FSCONV: Monaural Simple SRC**
 - 1ch x2
 - FSI = 44.1kHz to 48kHz , FSO = 8kHz to 16kHz (FSO/FSI = 0.167 to 0.363)
- **DIT:**
 - S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible
 - 24-bit Stereo Output
- **Digital Interface:**
 - Digital Input Port: max 24ch when TDM mode
 - Digital Output Port: max 28ch when TDM mode
 - Independent LRCK/BICK Input port x 5 Lines
 - Data Format: MSB 32,24-bit / LSB 24,20,16-bit / I²S
 - PCM Short / Long Frame Supported
 - TDM Format Supported
- **Digital Mixer Circuit**
- **PLL Circuit**
- **μP Interface: SPI(7MHz max), I²C-bus (1MHz, Fast Mode Plus)**
- **Power Supply:**
 - Analog AVDD: 3.0 to 3.6V (typ. 3.3V)
 - Digital LVDD: 3.0 to 3.6V (typ. 3.3V) (3.3V → 1.2V regulator integrated)
 - I/F VDD33: 3.0 to 3.6V (typ. 3.3V)
TVDD1: 1.7 to 3.6V (typ. 3.3V)
TVDD2: 1.7 to 3.6V (typ. 3.3V)
- **Operating Temperature Range: -40°C to 85°C**
- **Package: 64-pin LQFP (10mm x 10mm, 0.5mm pitch)**

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4. Block Diagram and Functions

■ Block Diagram

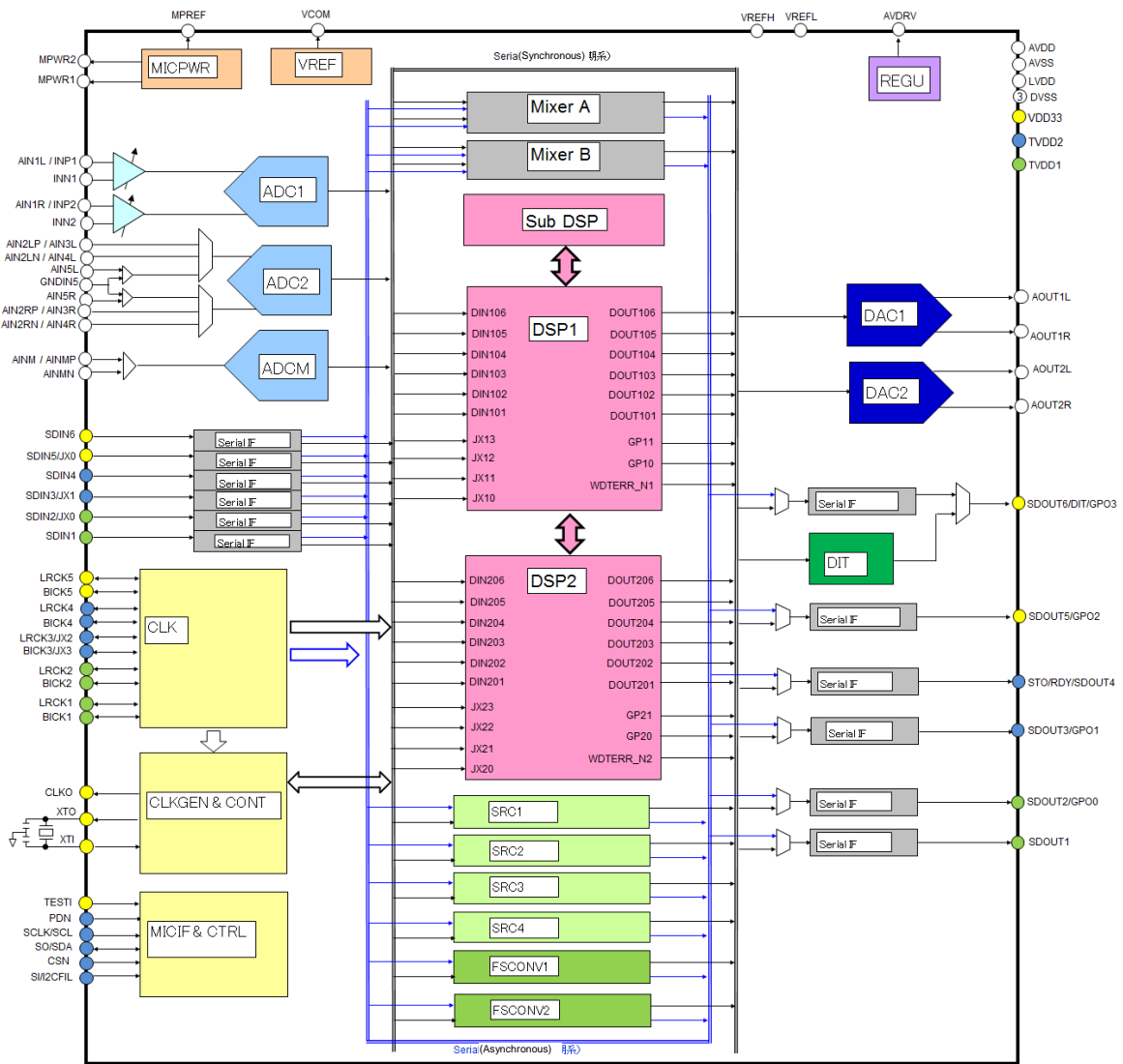


Figure 1. Block Diagram

■ DSP1 Block Diagram

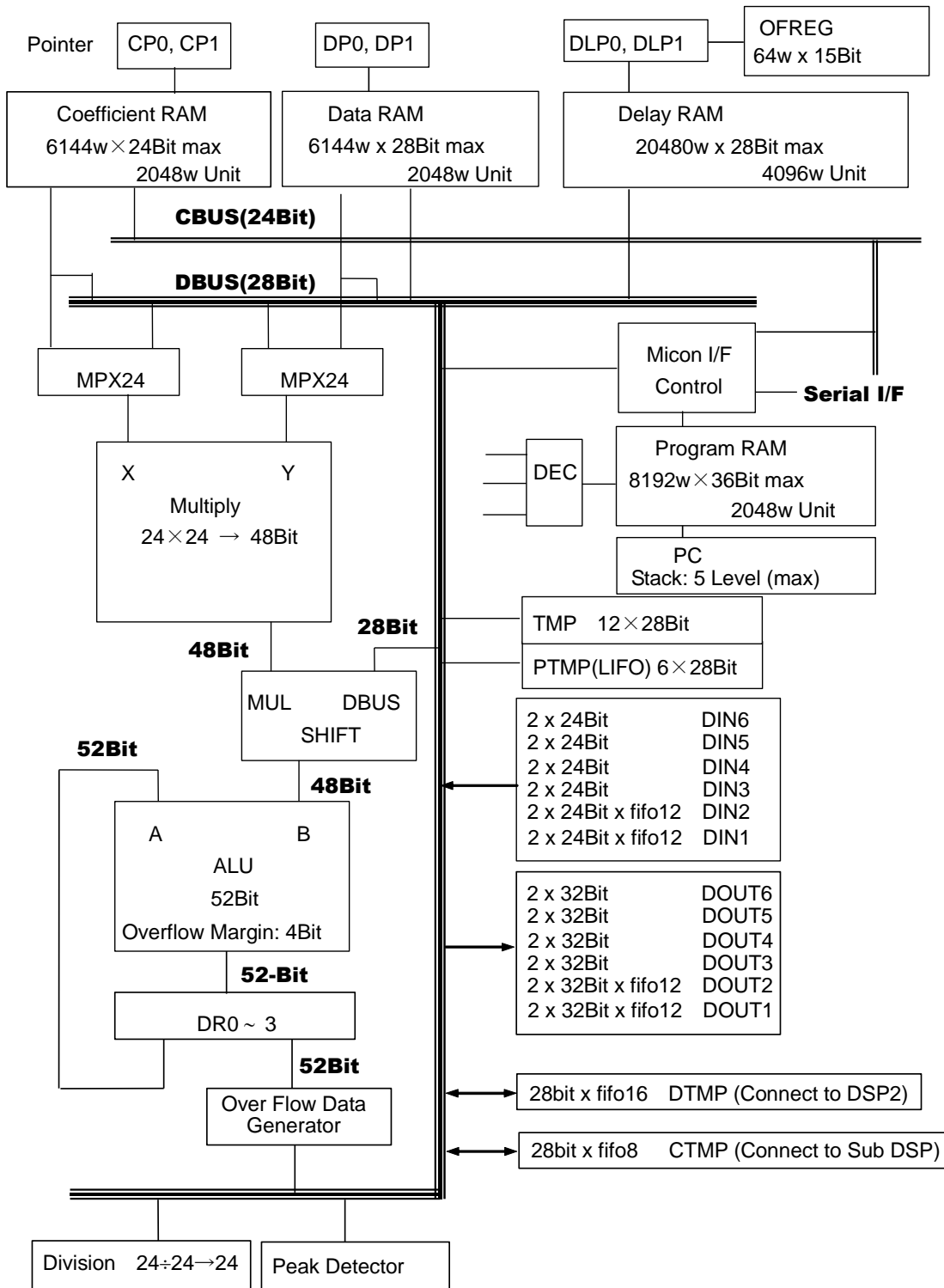


Figure 2. DSP1 Block Diagram (Note 1)

Note 1. Coefficient RAM, Data RAM, Delay RAM, Program RAM areas are shared by DSP1 and DSP2 and the sizes are configurable by control registers.

■ DSP2 Block Diagram

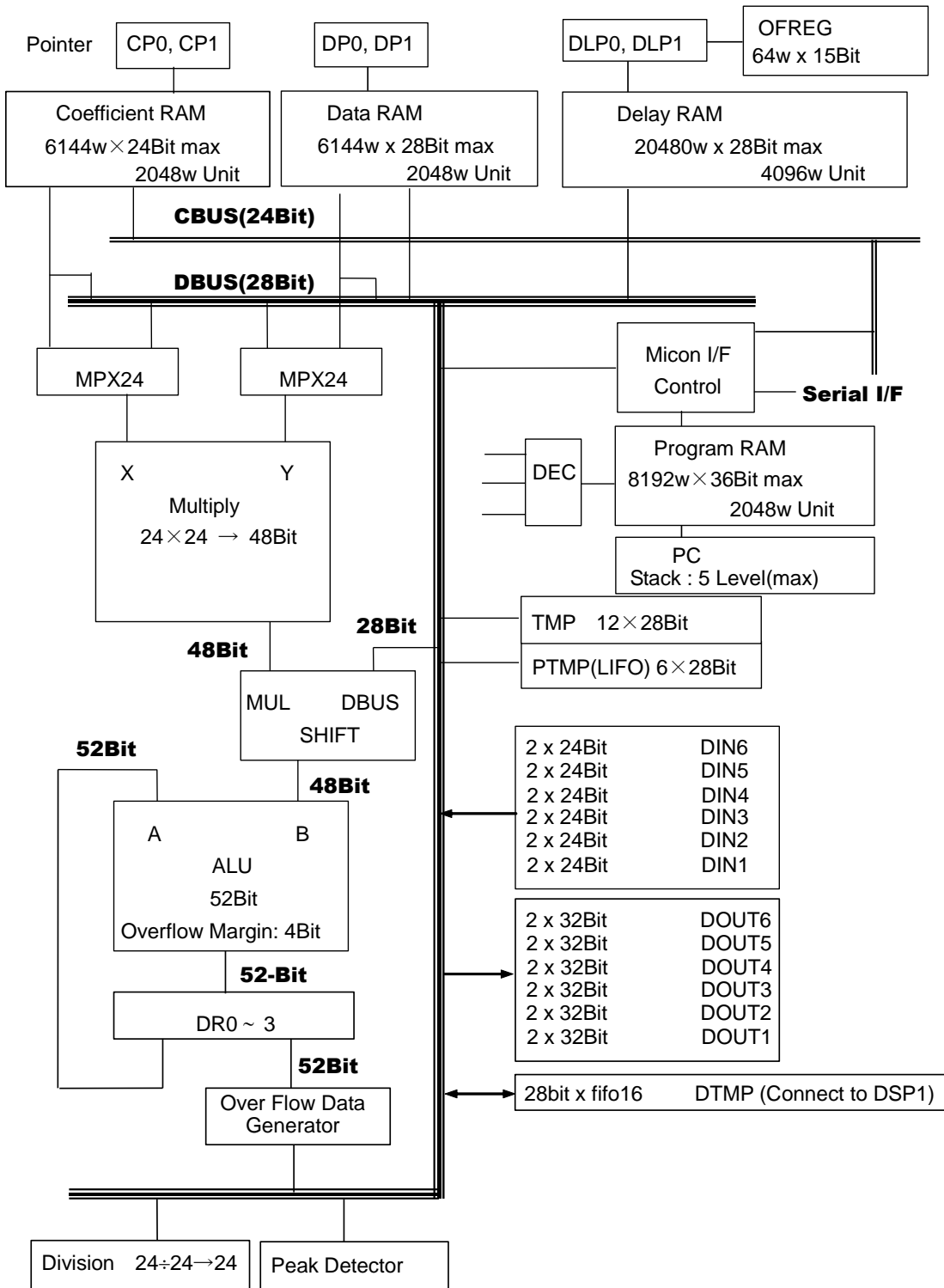


Figure 3. DSP2 Block Diagram (Note 1)

■ Sub DSP Block Diagram

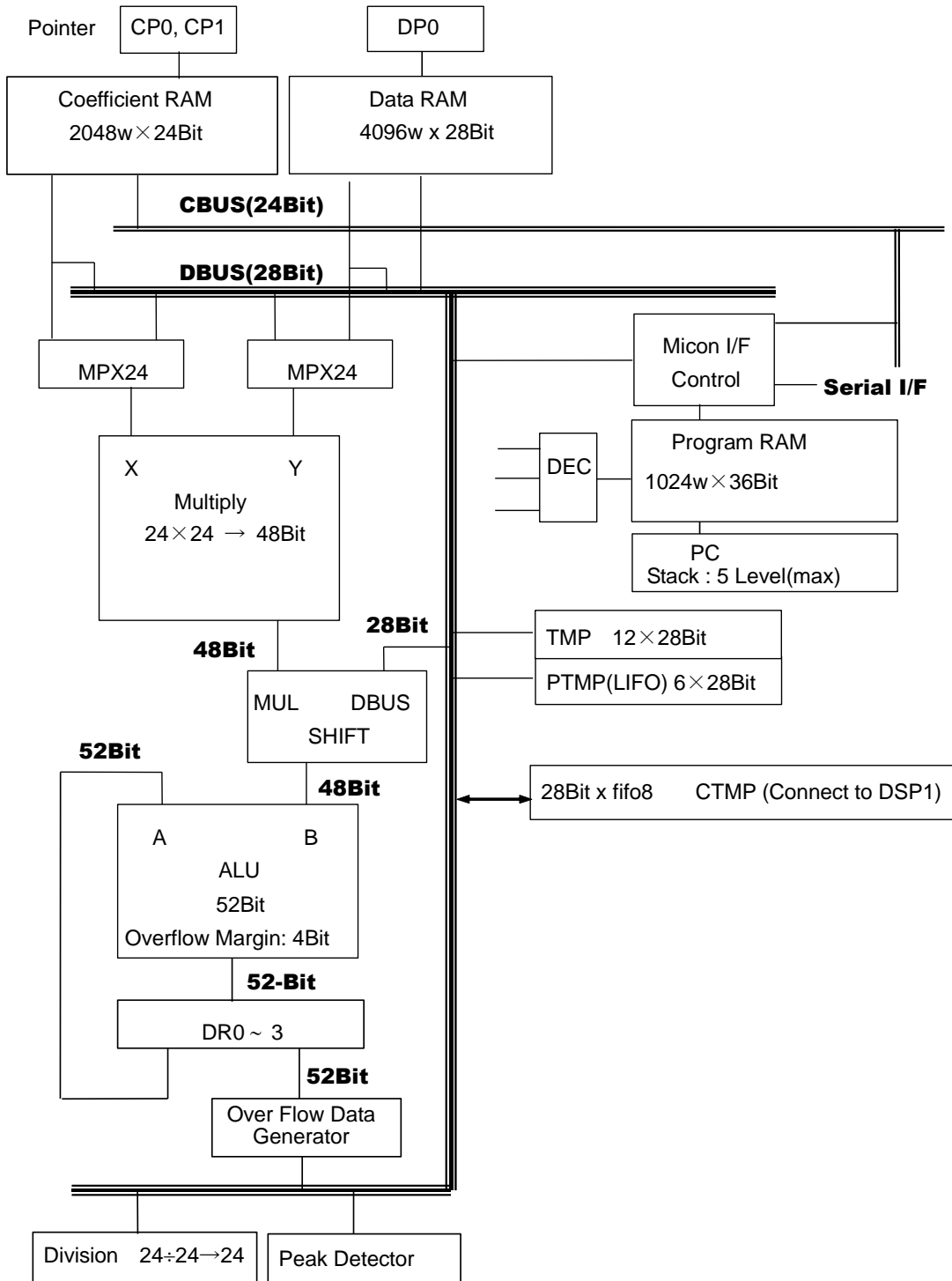


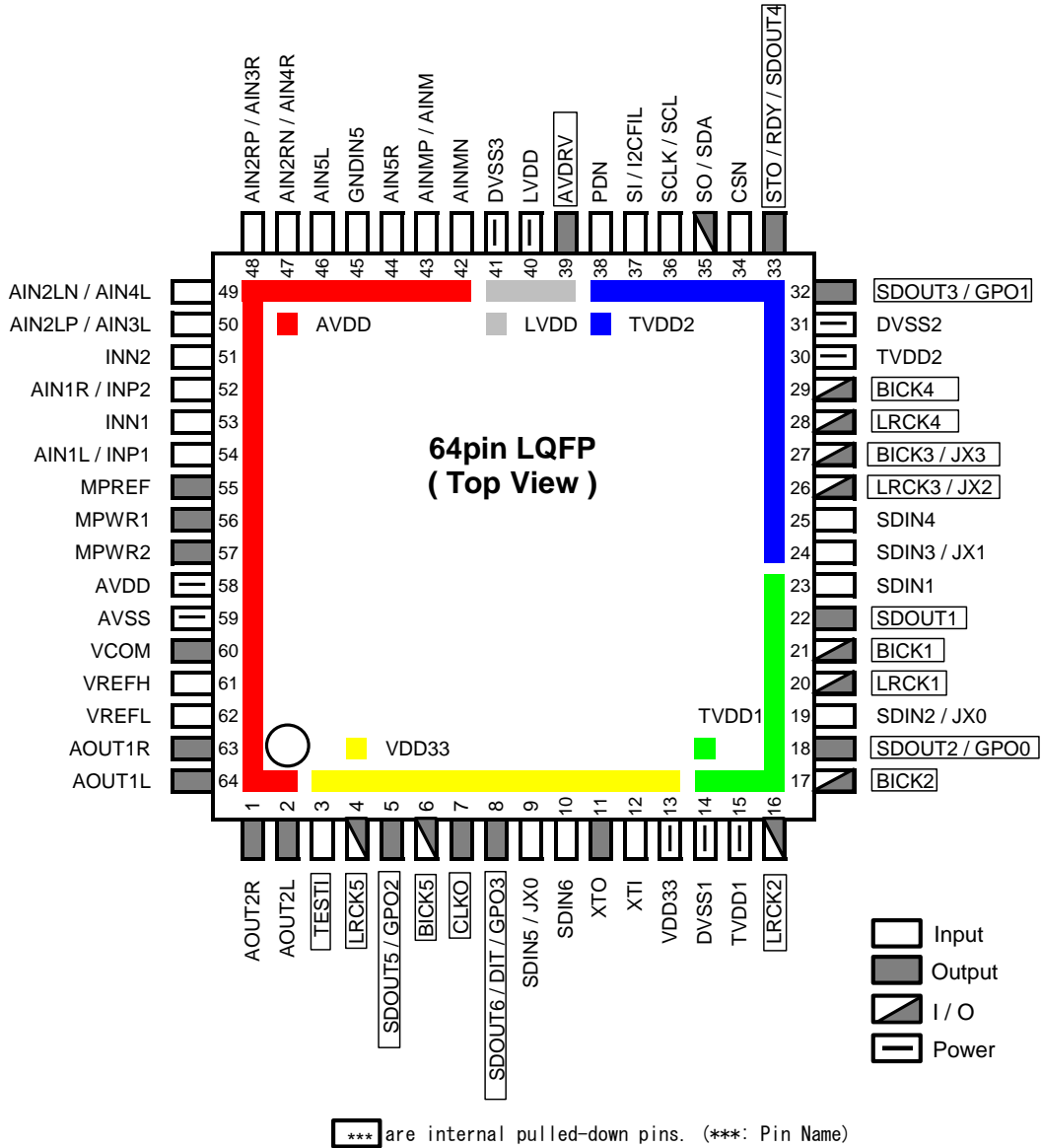
Figure 4. Sub DSP Block Diagram

5. Pin Configurations and Functions

Ordering Guide

AK7738VQ: -40 ~ +85°C 64-pin LQFP (0.5mm pitch)
 AKD7738: Evaluation Board for AK7738

Pin Layout



■ Pin Functions

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 1 | AOUT2R | O | DAC2 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state. |
| 2 | AOUT2L | O | DAC2 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state. |
| 3 | TESTI | I | Test Input Pin It must be tied "L". |
| 4 | LRCK5 | I/O | LR Channel Select Clock 5 Pin |
| 5 | SDOUT5 | O | Serial Data Output 5 Pin |
| | GPO2 | O | DSP Programmable Output 2 Pin (GPO0 Output of DSP2) |
| 6 | BICK5 | I/O | Serial Bit Clock 5 Pin |
| 7 | CLKO | O | Master Clock Output Pin |
| 8 | SDOUT6 | O | Serial Data Output 6 Pin |
| | DIT | O | Digital Transmit Channel Output Pin |
| | GPO3 | O | DSP Programmable Output 3 Pin (GPO1 Output of DSP2) |
| 9 | SDIN5 | I | Serial Data Input 5 Pin |
| | JX0 | I | External Conditional Jump Input 0 Pin |
| 10 | SDIN6 | I | Serial Data Input 6 Pin |
| 11 | XTO | O | Crystal Oscillator Output Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, leave this pin open. |
| 12 | XTI | I | Crystal Oscillator Input Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, connect this pin to an external clock or DVSS1. |
| 13 | VDD33 | - | Digital I/F Power Supply Pin 3.0~3.6V (typ.3.3V) |
| 14 | DVSS1 | - | Digital Ground 1 Pin 0V (Substrate potential) |
| 15 | TVDD1 | - | Digital I/F Power Supply 1 Pin 1.7~3.6V (typ.3.3V) |
| 16 | LRCK2 | I/O | LR Channel Select Clock 2 Pin |
| 17 | BICK2 | I/O | Serial Bit Clock 2 Pin |
| 18 | SDOUT2 | O | Serial Data Output 2 Pin |
| | GPO0 | O | DSP Programmable Output 0 Pin (GPO0 Output of DSP1) |
| 19 | SDIN2 | I | Serial Data Input 2 Pin |
| | JX0 | I | External Conditional Jump Input 0 Pin |
| 20 | LRCK1 | I/O | LR Channel Select Clock 1 Pin |
| 21 | BICK1 | I/O | Serial Bit Clock 1 Pin |
| 22 | SDOUT1 | O | Serial Data Output 1 Pin |
| 23 | SDIN1 | I | Serial Data Input 1 Pin |

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 24 | SDIN3 | I | Serial Data Input 3 Pin |
| | JX1 | I | External Conditional Jump Input 1 Pin |
| 25 | SDIN4 | I | Serial Data Input 4 Pin |
| 26 | LRCK3 | I/O | LR Channel Select Clock 3 Pin |
| | JX2 | I | External Conditional Jump Input 2 Pin |
| 27 | BICK3 | I/O | Serial Bit Clock 3 Pin |
| | JX3 | I | External Conditional Jump Input 3 Pin |
| 28 | LRCK4 | I/O | LR Channel Select Clock 4 Pin |
| 29 | BICK4 | I/O | Serial Bit Clock 4 Pin |
| 30 | TVDD2 | - | Digital I/F Power Supply 2 Pin 1.7~3.6V (typ.3.3V) |
| 31 | DVSS2 | - | Digital Ground 2 Pin 0V (Substrate potential) |
| 32 | SDOUT3 | O | Serial Data Output 3 Pin |
| | GPO1 | O | DSP Programmable Output 1 Pin (GPO1 Output of DSP1) |
| 33 | STO | O | Status Output Pin This pin outputs "L" during power-down state. |
| | RDY | O | RDY Signal Output Pin |
| | SDOUT4 | O | Serial Data Output 4 Pin |
| 34 | CSN | I | SPI Mode SPI I/F Chip Select N Pin During power-down state or when μ P I/F are not in use, leave this pin "H" level. |
| | | I | I ² C Mode I ² C I/F Chip Address N Pin This pin must be pulled up or pulled down. |
| 35 | SO | O | Serial Data Output Pin for SPI I/F This pin outputs "Hi-Z" during power-down state. |
| | SDA | I/O | Serial Data In/Output Pin for I ² C I/F This pin outputs "Hi-Z" during power-down state. |
| 36 | SCLK | I | Serial Data Clock Input Pin for SPI I/F |
| | SCL | I | Serial Data Clock Input Pin for I ² C I/F |
| 37 | SI | I | Serial Data Input Pin for SPI I/F |
| | I2CFIL | I | I ² C I/F Mode Select Input Pin I2CFIL = "L": Fast Mode (400kHz) I2CFIL = "H": Fast Mode Plus (1MHz) (should be fixed to TVDD2) |
| 38 | PDN | I | Power-down N Pin Use this pin to power down the AK7738. The PDN pin should be held "L" when power is supplied. |
| 39 | AVDRV | O | LDO Output Pin Connect a 2.2 μ F ceramic capacitor between this pin and DVSS3. Do not connect this pin to an external circuit. |
| 40 | LVDD | - | Digital Core Power Supply Pin 3.0~3.6V (typ.3.3V) |
| 41 | DVSS3 | - | Digital Ground 3 Pin 0V (Substrate potential) |

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 42 | AINMN | I | ADCM Inverted Differential Input Pin |
| 43 | AINMP | I | ADCM Non-inverted Differential Input Pin |
| | AINM | I | ADCM Single-ended Input Pin |
| 44 | AIN5R | I | ADC2 Rch Pseudo Differential Input 5 Pin |
| 45 | GNDIN5 | I | ADC2 Pseudo Differential Ground Input 5 Pin |
| 46 | AIN5L | I | ADC2 Lch Pseudo Differential Input 5 Pin |
| 47 | AIN2RN | I | ADC2 Rch Inverted Differential Input 2 Pin |
| | AIN4R | I | ADC2 Rch Single-ended Input 4 Pin |
| 48 | AIN2RP | I | ADC2 Rch Non-inverted Differential Input 2 Pin |
| | AIN3R | I | ADC2 Rch Single-ended Input 3 Pin |
| 49 | AIN2LN | I | ADC2 Lch Inverted Differential Input 2 Pin |
| | AIN4L | I | ADC2 Lch Single-ended Input 4 Pin |
| 50 | AIN2LP | I | ADC2 Lch Non-inverted Differential Input 2 Pin |
| | AIN3L | I | ADC2 Lch Single-ended Input 3 Pin |
| 51 | INN2 | I | ADC1 Rch Inverted Differential Input 2 Pin |
| 52 | AIN1R | I | ADC1 Rch Single-ended Input 1 Pin |
| | INP2 | I | ADC1 Rch Non-inverted Differential Input 2 Pin |
| 53 | INN1 | I | ADC1 Lch Inverted Differential Input 1 Pin |
| 54 | AIN1L | I | ADC1 Lch Single-ended Input 1 Pin |
| | INP1 | I | ADC1 Lch Non-inverted Differential Input 1 Pin |
| 55 | MPREF | O | Ripple Filter Pin for Microphone Power Supply Connect a 1uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. |
| 56 | MPWR1 | O | Power Supply Output 1 Pin for Microphone This pin outputs "Hi-Z" during power-down state. |
| 57 | MPWR2 | O | Power Supply Output 2 Pin for Microphone This pin outputs "Hi-Z" during power-down state. |
| 58 | AVDD | - | Analog Power Supply Pin 3.0~3.6V (typ.3.3V) |
| 59 | AVSS | - | Analog Ground Pin 0V (Substrate potential) |
| 60 | VCOM | O | Analog Common Voltage Output Pin Connect a 2.2uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. This pin outputs "L" during power-down state. |
| 61 | VREFH | I | Analog High-level Reference Voltage Input Pin Connect this pin to AVDD. |
| 62 | VREFL | I | Analog Low-level Reference Voltage Input Pin Connect this pin to AVSS. |
| 63 | AOUT1R | O | DAC1 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state. |
| 64 | AOUT1L | O | DAC1 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state. |

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

| Classification | Pin Name | Setting |
|----------------|--|----------------------|
| Analog | MPREF, MPWR1, MPWR2, AIN1L/INP1, INN1, AIN1R/INP2, INN2, AIN2LP/AIN3L, AIN2LN/AIN4L, AIN2RP/AIN3R, AIN2RN/AIN4R, AIN5L, GNDIN5, AIN5R, AINMP/AINM, AINMN, AOUT1L, AOUT1R, AOUT2L, AOUT2R | Open |
| Digital | CLKO, XTO, SDOUT1, SDOUT2/GPO0, SDOUT3/GPO1, STO/RDY/SDOUT4, SDOUT5/GPO2, SDOUT6/DIT/GPO3 | Open |
| | XTI, SDIN6, SDIN5/JX0, SDIN4, SDIN3/JX1, SDIN2/JX0, SDIN1, LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, LRCK5, BICK5, TESTI | Connect to DVSS1 ~ 3 |

Table 1. Handling of Unused Pins

Note 2. Although it is recommended that the LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, LRCK5 and BICK5 pins are connected to DVSS1-3 when not using, they can be open since they are pulled down internally.

■ Internal Pulled-down Pin Status

Internal pulled-down I/O pins have different statuses in power-down and power-down release statuses.

| No | Pin Name | I/O | Power Down Status PDN pin = "L" | Power Down Release PDN pin = "H" (when I/O pin = Input) | Power Down Release PDN pin = "H" (when I/O pin = Output) |
|----|-----------------|-----|------------------------------------|---|--|
| 3 | TESTI | I | Pulled-down (25kΩ) | Pulled-down (25kΩ) | Pulled-down (25kΩ) |
| 4 | LRCK5 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 5 | SDOUT5/GPO2 | O | Pulled-down (50kΩ) | Output | Output |
| 6 | BICK5 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 7 | CLKO | O | Pulled-down (50kΩ) | Output | Output |
| 8 | SDOUT6/DIT/GPO3 | O | Pulled-down (50kΩ) | Output | Output |
| 16 | LRCK2 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 17 | BICK2 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 18 | SDOUT2/GPO0 | O | Pulled-down (50kΩ) | Output | Output |
| 20 | LRCK1 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 21 | BICK1 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 22 | SDOUT1 | O | Pulled-down (50kΩ) | Output | Output |
| 26 | LRCK3/JX2 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 27 | BICK3/JX3 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 28 | LRCK4 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 29 | BICK4 | I/O | Pulled-down (50kΩ) | Pulled-down (46kΩ) | Output |
| 32 | SDOUT3/GPO1 | O | Pulled-down (50kΩ) | Output | Output |
| 33 | STO/RDY/SDOUT4 | O | Pulled-down (50kΩ) | Output | Output |
| 39 | AVDRV | O | Pulled-down (70Ω) | Output | Output |

Table 2. Internal Pulled-down Pin Status

■ Power-down Status of Output Pins

| No | Pin Name | I/O | Power-down Status | No | Pin Name | I/O | Power-down Status |
|----|-----------|-----|-------------------|----|-----------------|-----|-------------------|
| 60 | VCOM | O | “L” Output | 35 | SO/SDA | I/O | “Hi-Z” Output |
| 55 | MPREF | O | “L” Output | | | | |
| 56 | MPWR1 | O | “Hi-Z” Output | 22 | SDOUT1 | O | “L” Output |
| 57 | MPWR2 | O | “Hi-Z” Output | 18 | SDOUT2/GPO0 | O | “L” Output |
| 64 | AOUT1L | O | “Hi-Z” Output | 32 | SDOUT3/GPO1 | O | “L” Output |
| 63 | AOUT1R | O | “Hi-Z” Output | 33 | STO/RDY/SDOUT4 | O | “L” Output |
| 2 | AOUT2L | O | “Hi-Z” Output | 5 | SDOUT5/GPO2 | O | “L” Output |
| 1 | AOUT2R | O | “Hi-Z” Output | 8 | SDOUT6/DIT/GPO3 | O | “L” Output |
| 20 | LRCK1 | I/O | Input | 7 | CLKO | O | “L” Output |
| 21 | BICK1 | I/O | Input | 11 | XTO | O | “H” Output |
| 16 | LRCK2 | I/O | Input | 39 | AVDRV | O | “L” Output |
| 17 | BICK2 | I/O | Input | | | | |
| 26 | LRCK3/JX2 | I/O | Input | | | | |
| 27 | BICK3/JX3 | I/O | Input | | | | |
| 28 | LRCK4 | I/O | Input | | | | |
| 29 | BICK4 | I/O | Input | | | | |
| 4 | LRCK5 | I/O | Input | | | | |
| 6 | BICK5 | I/O | Input | | | | |

Table 3. Power-down Status of Output Pins

■ Relationship between Power Supplies and Digital Pins

| Power Supply | Digital Pins |
|--------------|--|
| TVDD1 | SDIN1, SDIN2/JX0, SDOUT1, SDOUT2/GPO0, LRCK1, BICK1, LRCK2, BICK2 |
| TVDD2 | SDIN3/JX1, SDIN4, SDOUT3/GPO1, STO/RDY/SDOUT4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN, SI/I2CFIL |
| VDD33 | SDIN5/JX0, SDIN6, SDOUT5/GPO2, SDOUT6/DIT/GPO3, LRCK5, BICK5, CLKO, TESTI, XTO, XTI |

Table 4. Relationship between Power Supplies and Digital Pins

6. Absolute Maximum Ratings

(AVSS=DVSS1=DVSS2=DVSS3=0V; Note 3)

| Parameter | Symbol | min | max | Unit |
|--|--------|------|-----------------|------|
| Power Supplies | | | | |
| Analog | AVDD | -0.3 | 4.3 | V |
| Digital1(Core) | LVDD | -0.3 | 4.3 | V |
| Digital2(I/F) | TVDD1 | -0.3 | 4.3 | V |
| Digital3(I/F) | TVDD2 | -0.3 | 4.3 | V |
| Digital4(I/F) | VDD33 | -0.3 | 4.3 | V |
| DVSS-AVSS (Note 3) | ΔGND | -0.3 | 0.3 | V |
| Input Current (except power supply pins) | IIN | — | ±10 | mA |
| Analog Input Voltage (Note 4) | VINA | -0.3 | (AVDD+0.3)≤4.3 | V |
| Digital Input Voltage (Note 5) | VIND1 | -0.3 | (TVDD1+0.3)≤4.3 | V |
| Digital Input Voltage (Note 6) | VIND2 | -0.3 | (TVDD2+0.3)≤4.3 | V |
| Digital Input Voltage (Note 7) | VIND3 | -0.3 | (VDD33+0.3)≤4.3 | V |
| Ambient Temperature (Power applied) | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 3. All voltages are with respect to ground. AVSS and DVSS1-3 must be connected to the same ground.

Note 4. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.

Note 5. The maximum digital input voltage of SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2 and BICK2 pins is smaller value between (TVDD1+0.3)V and 4.3V.

Note 6. The maximum digital input voltage of SDIN3/JX1, SDIN4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN and SI/I2CFIL pins is smaller value between (TVDD2+0.3)V and 4.3V.

Note 7. The maximum digital input voltage of SDIN5/JX0, SDIN6, LRCK5, BICK5, TESTI and XTI pins is smaller value between (VDD33+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS1=DVSS2=DVSS3=0V; Note 3)

| Parameter | Symbol | min | typ | max | Unit |
|-----------------------|--------|-----|-----|-----|------|
| Power Supplies | | | | | |
| Analog | AVDD | 3.0 | 3.3 | 3.6 | V |
| Digital1(Core) | LVDD | 3.0 | 3.3 | 3.6 | V |
| Digital2(I/F) | TVDD1 | 1.7 | 3.3 | 3.6 | V |
| Digital3(I/F) | TVDD2 | 1.7 | 3.3 | 3.6 | V |
| Digital4(I/F) | VDD33 | 3.0 | 3.3 | 3.6 | V |

Note 8. The power-up sequence with AVDD, DVDD, TVDD1, TVDD2 and VDD33 is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

Note 9. Do not turn off the power supply of the AK7738 with the power supply of the peripheral device turned on. When using the I²C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD2 or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP Gain

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V)

| Parameter | | min | typ | max | Unit | |
|------------------------------------|-----------------|------------------------------------|-----|-----|------|----|
| MIC AMP | Input Impedance | 14 | 20 | 26 | kΩ | |
| | Gain | MGNL[3:0]bits=0h, MGNR[3:0]bits=0h | -1 | 0 | 1 | dB |
| | | MGNL[3:0]bits=1h, MGNR[3:0]bits=1h | 1 | 2 | 3 | |
| | | MGNL[3:0]bits=2h, MGNR[3:0]bits=2h | 3 | 4 | 5 | |
| | | MGNL[3:0]bits=3h, MGNR[3:0]bits=3h | 5 | 6 | 7 | |
| | | MGNL[3:0]bits=4h, MGNR[3:0]bits=4h | 7 | 8 | 9 | |
| | | MGNL[3:0]bits=5h, MGNR[3:0]bits=5h | 9 | 10 | 11 | |
| | | MGNL[3:0]bits=6h, MGNR[3:0]bits=6h | 11 | 12 | 13 | |
| | | MGNL[3:0]bits=7h, MGNR[3:0]bits=7h | 13 | 14 | 15 | |
| | | MGNL[3:0]bits=8h, MGNR[3:0]bits=8h | 15 | 16 | 17 | |
| | | MGNL[3:0]bits=9h, MGNR[3:0]bits=9h | 17 | 18 | 19 | |
| | | MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah | 20 | 21 | 22 | |
| | | MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh | 23 | 24 | 25 | |
| | | MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch | 26 | 27 | 28 | |
| | | MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh | 29 | 30 | 31 | |
| MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh | 32 | 33 | 34 | | | |
| MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh | 35 | 36 | 37 | | | |

2. MIC Bias

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;

Measurement Frequency =20Hz~20kHz)

| Parameter | | min | typ | max | Unit |
|-----------|---------------------------|-----|------|------|------|
| MIC Bias | Output Voltage | 2.3 | 2.5 | 2.7 | V |
| | Load Resistance | 2 | | | kΩ |
| | Load Capaitance | | | 30 | pF |
| | Output Noise (A-weighted) | | -114 | -108 | dBV |
| | | | | | |

3. MIC AMP + ADC1

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data; BICK=64fs, Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

| | Parameter | | min | typ | max | Unit |
|--|----------------------------|---------------------------------|--------|--------|--------|-----------------|
| | | Resolution | | | | 24 |
| MIC AMP + ADC1 | Input Voltage (Note 13) | Differential Input (Note 11) | ±2.1 | ±2.3 | ±2.5 | V _{pp} |
| | | Differential Input (Note 12) | ±0.264 | ±0.290 | ±0.315 | |
| | | Single-ended Input (Note 11) | 2.1 | 2.3 | 2.5 | V _{pp} |
| | | Single-ended Input (Note 12) | 0.264 | 0.290 | 0.315 | |
| | S/(N+D) (-1dBFS) | fs=48kHz (Note 11) | 80 | 90 | | dB |
| | | fs=48kHz (Note 12) | | 82 | | |
| | | fs=96kHz (Note 11) | | 87 | | |
| | | fs=96kHz (Note 12) | | 79 | | |
| | | fs=192kHz (Note 11, Note 14) | | 87 | | |
| | | fs=192kHz (Note 12, Note 14) | | 79 | | |
| | Dynamic Range (-60dBFS) | fs=48kHz (A-weighted) (Note 11) | 94 | 102 | | dB |
| | | fs=48kHz (A-weighted) (Note 12) | | 90 | | |
| | | fs=96kHz (Note 11) | | 95 | | |
| | | fs=96kHz (Note 12) | | 87 | | |
| | | fs=192kHz (Note 11) | | 95 | | |
| | | fs=192kHz (Note 12) | | 87 | | |
| | S/N | fs=48kHz (A-weighted) (Note 11) | 94 | 102 | | dB |
| | | fs=48kHz (A-weighted) (Note 12) | | 90 | | |
| | | fs=96kHz (Note 11) | | 95 | | |
| | | fs=96kHz (Note 12) | | 87 | | |
| fs=192kHz (Note 11) | | | 95 | | | |
| fs=192kHz (Note 12) | | | 87 | | | |
| Inter-Channel Isolation (fin=1kHz) (Note 10) | | 90 | 105 | | dB | |
| Channel Gain Mismatch | | | 0.0 | 0.3 | dB | |

Note 10. Inter-channel isolation with -1dBFS signal input.

Note 11. MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is proportional to AVDD (0.7 x AVDD).

Note 12. MGNL/R[3:0] bits = 9h (+18dB). Input full-scale voltage is proportional to AVDD (0.088 x AVDD).

Note 13. -0.7dBFS is output when fs=192kHz and ADC1 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

Note 14. In the case of inputting -1.6dBFS when fs=192kHz and ADC1 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

4. ADC2

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

| ADC2 | Parameter | min | typ | max | Unit |
|----------------------------|--|------------|------|------|-----------------|
| | | Resolution | | | 24 |
| | Input Impedance | 14 | 20 | 26 | kΩ |
| Input Voltage (Note 18) | Differential Input (Note 15) | ±2.1 | ±2.3 | ±2.5 | V _{pp} |
| | Single-ended Input (Note 16) | 2.1 | 2.3 | 2.5 | V _{pp} |
| | Pseudo Differential Input (Note 17) | 2.1 | 2.3 | 2.5 | V _{pp} |
| S/(N+D) (-1dBFS) | fs=48kHz | 80 | 90 | | dB |
| | fs=96kHz | | 87 | | |
| | fs=192kHz (Note 19) | | 87 | | |
| Dynamic Range (-60dBFS) | fs=48kHz (A-weighted) | 94 | 102 | | dB |
| | fs=96kHz | | 95 | | |
| | fs=192kHz | | 95 | | |
| S/N | fs=48kHz (A-weighted) | 94 | 102 | | dB |
| | fs=96kHz | | 95 | | |
| | fs=192kHz | | 95 | | |
| | Inter-Channel Isolation (fin=1kHz) (Note 10) | 90 | 105 | | dB |
| | Channel Gain Mismatch | | 0.0 | 0.3 | dB |

Note 15. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins.

Note 16. AIN3L, AIN3R, AIN4L and AIN4R pins.

Note 17. AIN5L and AIN5R pins.

Note 18. -0.7dBFS is output when fs=192kHz and ADC2 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

Note 19. In the case of inputting -1.6dBFS when fs=192kHz and ADC2 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

5. ADCM

(Ta=25°C; AVDD=LVD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

| ADCM | Parameter | min | typ | max | Unit |
|----------------------------|------------------------------|------|------|------|------|
| | Resolution | | | | 24 |
| Input Impedance | | 14 | 20 | 26 | kΩ |
| Input Voltage (Note 22) | Differential Input (Note 20) | ±2.1 | ±2.3 | ±2.5 | Vpp |
| | Single-ended Input (Note 21) | 2.1 | 2.3 | 2.5 | Vpp |
| S/(N+D) (-1dBFS) | fs=48kHz | 80 | 90 | | dB |
| | fs=96kHz | | 87 | | |
| | fs=192kHz (Note 23) | | 87 | | |
| Dynamic Range (-60dBFS) | fs=48kHz (A-weighted) | 94 | 102 | | dB |
| | fs=96kHz | | 95 | | |
| | fs=192kHz | | 95 | | |
| S/N | fs=48kHz (A-weighted) | 94 | 102 | | dB |
| | fs=96kHz | | 95 | | |
| | fs=192kHz | | 95 | | |

Note 20. AINMP and AINMN pins.

Note 21. AINM pin.

Note 22. -0.7dBFS is output when fs=192kHz and ADCM digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

Note 23. In the case of inputting -1.6dBFS when fs=192kHz and ADCM digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

6. DAC

(Ta=25°C; AVDD= LVDD =TVDD1=TVDD2= VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 32-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz; Unless otherwise specified.)

| DAC1 DAC2 | Parameter | min | typ | max | Unit |
|------------------------------------|-----------------------|------|------|------|------|
| | Resolution | | | | 32 |
| Output Voltage | (Note 24) | 2.55 | 2.83 | 3.11 | Vpp |
| S/(N+D) (0dBFS) | fs=48kHz | 80 | 91 | | dB |
| | fs=96kHz | | 89 | | |
| | fs=192kHz | | 89 | | |
| Dynamic Range (-60dBFS) | fs=48kHz (A-weighted) | 100 | 108 | | dB |
| | fs=96kHz | | 101 | | |
| | fs=192kHz | | 101 | | |
| S/N | fs=48kHz (A-weighted) | 100 | 108 | | dB |
| | fs=96kHz | | 101 | | |
| | fs=192kHz | | 101 | | |
| Inter-Channel Isolation (fin=1kHz) | (Note 25) | 90 | 110 | | dB |
| Channel Gain Mismatch | | | 0.0 | 0.7 | dB |
| Load Resistance | (Note 26) | 10 | | | kΩ |
| Load Capacitance | | | | 30 | pF |

Note 24. The output voltage when 0dBFS signal input. The output voltage is proportional to AVDD (AVDD x 0.86).

Note 25. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, and AOUT2L and AOUT2R)

Note 26. to AC load

7. SRC

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V;
Signal Frequency=1kHz; 24-bit Data; Measurement Frequency=20Hz ~ FSO/2)

| Parameter | Symbol | min | typ | max | Unit | | |
|--|-------------------------------------|------------------------|------|------------------|------|--|----|
| Resolution | | | | 24 | Bit | | |
| Input Sample Rate | FSI | 8 | | 192 (Note 27) | kHz | | |
| Output Sample Rate | FSO | 8 | | 192 | kHz | | |
| THD+N (Input=1kHz, 0dBFS) | FSO/FSI=192kHz/48kHz | | -113 | -103 | dB | | |
| | FSO/FSI=192kHz/44.1kHz | | -113 | | dB | | |
| | FSO/FSI=44.1kHz/48kHz | | -112 | | dB | | |
| | FSO/FSI=44.1kHz/96kHz | | -111 | | dB | | |
| | FSO/FSI=48kHz/44.1kHz | | -112 | | dB | | |
| | FSO/FSI=48kHz/96kHz | | -113 | | dB | | |
| | FSO/FSI=48kHz/8kHz | | -111 | | dB | | |
| | FSO/FSI=16kHz/48kHz | | -113 | | dB | | |
| | FSO/FSI=16kHz/44.1kHz | | -100 | | dB | | |
| | FSO/FSI=8kHz/48kHz | | -113 | | dB | | |
| | FSO/FSI=8kHz/44.1kHz | | -95 | | dB | | |
| | FSO/FSI=48kHz/192kHz | | -105 | | dB | | |
| | FSO/FSI=44.1kHz/192kHz | | -102 | | dB | | |
| | Dynamic Range (Input=1kHz, -60dBFS) | FSO/FSI=192kHz/48kHz | | | 113 | | dB |
| | | FSO/FSI=192kHz/44.1kHz | | | 113 | | dB |
| | | FSO/FSI=44.1kHz/48kHz | | | 113 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | 113 | | dB | | |
| FSO/FSI=48kHz/44.1kHz | | 108 | 113 | | dB | | |
| FSO/FSI=48kHz/96kHz | | | 113 | | dB | | |
| FSO/FSI=48kHz/8kHz | | | 113 | | dB | | |
| FSO/FSI=16kHz/48kHz | | | 113 | | dB | | |
| FSO/FSI=16kHz/44.1kHz | | | 113 | | dB | | |
| FSO/FSI=8kHz/48kHz | | | 111 | | dB | | |
| FSO/FSI=8kHz/44.1kHz | | | 114 | | dB | | |
| FSO/FSI=48kHz/192kHz | | | 111 | | dB | | |
| FSO/FSI=44.1kHz/192kHz | | 110 | | dB | | | |
| Dynamic Range (Input=1kHz, -60dBFS, A-weighted) | | | | | | | |
| | FSO/FSI=44.1kHz/48kHz | | 115 | | dB | | |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.167 | | 6 | - | | |

Note 27. Set FSI frequency of each operating SRC as the sum of the frequencies is below 384kHz. For example, if the frequency of FSI is 96kHz, four SRCs can operate at the same time, if the frequency of FSI is 192kHz, only two SRCs are allowed to operate at the same time.

8. FSCONV

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V;
Signal Frequency=1kHz; 24-bit Data; Measurement Frequency=20Hz ~ FSO/2)

| FSCONV | Parameter | Symbol | min | typ | max | Unit |
|--|-------------------------------------|--------|------|------|-------|------|
| | Resolution | | | | 24 | Bit |
| | Input Sample Rate | FSI | 44.1 | | 48 | kHz |
| | Output Sample Rate | FSO | 8 | | 16 | kHz |
| | THD+N (Input=1kHz, 0dBFS) | | | | | |
| | FSO/FSI=16kHz/48kHz | | | -114 | | dB |
| | FSO/FSI=16kHz/44.1kHz | | | -95 | | dB |
| | FSO/FSI=8kHz/48kHz | | | -115 | | dB |
| | FSO/FSI=8kHz/44.1kHz | | | -97 | | dB |
| | Dynamic Range (Input=1kHz, -60dBFS) | | | | | |
| FSO/FSI=16kHz/48kHz | | | 114 | | dB | |
| FSO/FSI=16kHz/44.1kHz | | | 114 | | dB | |
| FSO/FSI=8kHz/48kHz | | | 114 | | dB | |
| FSO/FSI=8kHz/44.1kHz | | | 114 | | dB | |
| Dynamic Range (Input=1kHz, -60dBFS, A-weighted) | | | | | | |
| FSO/FSI=8kHz/48kHz | | | 117 | | dB | |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.167 | | | 0.363 | - |

■ Power Consumption

(Ta=25°C; AVDD=3.0~3.6V(typ=3.3V, max=3.6V); LVDD=3.0~3.6V(typ=3.3V, max=3.6V);
TVDD1=1.7~3.6V(typ=3.3V, max=3.6V); TVDD2=1.7~3.6V (typ=3.3V, max=3.6V); VDD33=3.0~3.6V
(typ=3.3V, max=3.6V); AVSS= DVSS1=DVSS2=DVSS3=0V; fs=192kHz; BICK=64fs;
SDOUT1~6/LRCK1~5/BICK1~5=Output; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|--------------------------------------|--------|-----|------|-----|------|
| Power-Up (PDN pin= "H") (Note 28) | AVDD | | 26 | 37 | mA |
| | LVDD | | 70 | 140 | mA |
| | TVDD1 | | 1.6 | 2.4 | mA |
| | TVDD2 | | 1.6 | 2.4 | mA |
| | VDD33 | | 4 | 6 | mA |
| Power-Down (PDN pin= "L") | AVDD | | 0.01 | | mA |
| | LVDD | | 0.01 | | mA |
| | TVDD1 | | 0.01 | | mA |
| | TVDD2 | | 0.01 | | mA |
| | VDD33 | | 0.01 | | mA |

Note 28. The current of LVDD changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics

1. ADC Block

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V;
VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1-1 Sharp Roll-Off Filter (ADSD bit = "0", ADSL bit = "0")

fs=48kHz

| Parameter | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|------|------|------|------|
| SHARP ROLL-OFF | | | | | |
| Passband (Note 29) | 0dB ~ -0.06dB | PB | 0 | 22.1 | kHz |
| | -6.0dB | PB | 24.4 | | kHz |
| Stopband (Note 29) | SB | 27.8 | | | kHz |
| Stopband Attenuation | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~20kHz | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 30) | GD | | 19 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | |
| Frequency Response | -3.0dB | FR | 1.0 | | Hz |

fs=96kHz

| Parameter | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|------|------|------|------|
| SHARP ROLL-OFF | | | | | |
| Passband (Note 29) | 0dB ~ -0.06dB | PB | 0 | 44.2 | kHz |
| | -6.0dB | PB | 48.7 | | kHz |
| Stopband (Note 29) | SB | 55.6 | | | kHz |
| Stopband Attenuation | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 30) | GD | | 19 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | |
| Frequency Response | -3.0dB | FR | 1.9 | | Hz |

fs=192kHz

| Parameter | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|-------|-------|------|------|
| SHARP ROLL-OFF | | | | | |
| Passband (Note 29) | 0dB ~ -0.04dB | PB | 0 | 83.7 | kHz |
| | -6.0dB | PB | 100.1 | | kHz |
| Stopband (Note 29) | SB | 122.9 | | | kHz |
| Stopband Attenuation | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 30) | GD | | 15 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | |
| Frequency Response | -3.0dB | FR | 3.9 | | Hz |

1-2 Slow Roll-Off Filter (ADSD bit = “0”, ADSL bit = “1”)

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|----------------|-------------|------|------|------|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.074dB | PB | 0 | | 12.5 | kHz |
| | -6.0dB | PB | | 21.9 | | kHz |
| Stopband (Note 29) | | SB | 36.5 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~20kHz | | Δ GD | | 0 | | 1/fs |
| Group Delay (Note 30) | | GD | | 7 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.0 | | Hz |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|----------------|-------------|-----|------|-----|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.074dB | PB | 0 | | 25 | kHz |
| | -6.0dB | PB | | 43.7 | | kHz |
| Stopband (Note 29) | | SB | 73 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | 0 | | 1/fs |
| Group Delay (Note 30) | | GD | | 7 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.9 | | Hz |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|--------------|-------------|-----|------|------|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.7dB | PB | 0 | | 49.9 | kHz |
| | -6.0dB | PB | | 79.9 | | kHz |
| Stopband (Note 29) | | SB | 146 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | 0 | | 1/fs |
| Group Delay (Note 30) | | GD | | 8 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 3.88 | | Hz |

1-3 Short Delay Sharp Roll-Off Filter (ADSD bit = "1", ADSL bit = "0")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|-------------|------|------|------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.06dB | PB | 0 | | 22.1 | kHz |
| | -6.0dB | PB | | 24.4 | | kHz |
| Stopband (Note 29) | | SB | 27.8 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~20kHz | | Δ GD | | | 2.6 | 1/fs |
| Group Delay (Note 30) | | GD | | 5 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.0 | | Hz |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|-------------|------|------|------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.06dB | PB | 0 | | 44.2 | kHz |
| | -6.0dB | PB | | 48.7 | | kHz |
| Stopband (Note 29) | | SB | 55.6 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | | 2.6 | 1/fs |
| Group Delay (Note 30) | | GD | | 5 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.9 | | Hz |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|---------------|-------------|-------|-------|------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.04dB | PB | 0 | | 83.7 | kHz |
| | -6.0dB | PB | | 100.1 | | kHz |
| Stopband (Note 29) | | SB | 122.9 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | | 0.2 | 1/fs |
| Group Delay (Note 30) | | GD | | 6 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 3.88 | | Hz |

1-4 Short Delay Slow Roll-Off Filter (ADSD bit = "1", ADSL bit = "1")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|----------------|-------------|------|------|------|------|
| SHORT DELAY SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.074dB | PB | 0 | | 12.5 | kHz |
| | -6.0dB | PB | | 21.9 | | kHz |
| Stopband (Note 29) | | SB | 36.5 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~20kHz | | Δ GD | | | 2.6 | 1/fs |
| Group Delay (Note 30) | | GD | | 5 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.0 | | Hz |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|----------------|-------------|-----|------|-----|------|
| SHORT DELAY SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.074dB | PB | 0 | | 25 | kHz |
| | -6.0dB | PB | | 43.7 | | kHz |
| Stopband (Note 29) | | SB | 73 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | | 2.6 | 1/fs |
| Group Delay (Note 30) | | GD | | 5 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 1.9 | | Hz |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|------------------------------------|--------------|-------------|-------|------|------|------|
| SHORT DELAY SLOW ROLL-OFF | | | | | | |
| Passband (Note 29) | 0dB ~ -0.7dB | PB | 0 | | 49.9 | kHz |
| | -6.0dB | PB | | 77.7 | | kHz |
| Stopband (Note 29) | | SB | 145.9 | | | kHz |
| Stopband Attenuation | | SA | 85 | | | dB |
| Group Delay Distortion : 0Hz~40kHz | | Δ GD | | | 0.5 | 1/fs |
| Group Delay (Note 30) | | GD | | 6 | | 1/fs |
| ADC Digital Filter(HPF) | | | | | | |
| Frequency Response | -3.0dB | FR | | 3.88 | | Hz |

Note 29. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included.

Note 30. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register.

2. DAC Block

(Ta= 25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V;
VDD3=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

2-1 Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.08dB~+0.08dB | PB | 0 | | 22.2 | kHz |
| | -6.0dB | PB | | 23.99 | | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 31) | | SB | 26.2 | | | kHz |
| Stopband Attenuation | | SA | 69.9 | | | dB |
| Group Delay (Note 32) | | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 20kHz | | FR | -0.20 | | 0.10 | dB |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.08dB~+0.08dB | PB | 0 | | 44.4 | kHz |
| | -6.0dB | PB | | 48.00 | | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 31) | | SB | 52.5 | | | kHz |
| Stopband Attenuation | | SA | 69.8 | | | dB |
| Group Delay (Note 32) | | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 40kHz | | FR | -0.50 | | 0.10 | dB |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.08dB~+0.08dB | PB | 0 | | 88.8 | kHz |
| | -6.0dB | PB | | 96.00 | | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 31) | | SB | 104.9 | | | kHz |
| Stopband Attenuation | | SA | 69.8 | | | dB |
| Group Delay (Note 32) | | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 80kHz | | FR | -2.00 | | -0.00 | dB |

2-2 Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-------------------|--------|-------|-------|--------|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~ +0.021dB | PB | 0 | | 9.0 | kHz |
| | -3.0dB | PB | | 19.75 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.021 | dB |
| Stopband | (Note 31) | SB | 42.6 | | | kHz |
| Stopband Attenuation | (Note 33) | SA | 72.6 | | | dB |
| Group Delay | (Note 32) | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 20kHz | | FR | -3.75 | | -2.75 | dB |

fs=96kHz

| Parameter | | Symbol | Min | typ | max | Unit |
|----------------------------------|------------------|--------|-------|------|--------|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.023dB | PB | 0 | | 18.1 | kHz |
| | -3.0dB | PB | | 39.6 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.023 | dB |
| Stopband | (Note 31) | SB | 85.1 | | | kHz |
| Stopband Attenuation | (Note 33) | SA | 72.6 | | | dB |
| Group Delay | (Note 32) | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 40kHz | | FR | -4.25 | | -2.75 | dB |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|------------------|--------|-------|------|--------|------|
| SLOW ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.023dB | PB | 0 | | 36.1 | kHz |
| | -3.0dB | PB | | 79.3 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.023 | dB |
| Stopband | (Note 31) | SB | 170.3 | | | kHz |
| Stopband Attenuation | (Note 33) | SA | 72.6 | | | dB |
| Group Delay | (Note 32) | GD | | 26.4 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 80kHz | | FR | -5.00 | | -3.00 | dB |

2-3 Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.07dB | PB | 0 | | 22.0 | kHz |
| | -6.0dB | PB | | 24.11 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.07 | dB |
| Stopband (Note 31) | | SB | 26.2 | | | kHz |
| Stopband Attenuation | | SA | 56.6 | | | dB |
| Group Delay (Note 32) | | GD | | 5.9 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 20kHz | | FR | -0.20 | | 0.10 | dB |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.08dB~+0.08dB | PB | 0 | | 44.3 | kHz |
| | -6.0dB | PB | | 48.25 | | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 31) | | SB | 52.5 | | | kHz |
| Stopband Attenuation | | SA | 56.4 | | | dB |
| Group Delay (Note 32) | | GD | | 5.9 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 40kHz | | FR | -0.50 | | 0.10 | dB |

fs=192kHz

| Parameter | | Symbol | Min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.08dB~+0.08dB | PB | 0 | | 88.6 | kHz |
| | -6.0dB | PB | | 96.50 | | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 31) | | SB | 104.9 | | | kHz |
| Stopband Attenuation | | SA | 56.4 | | | dB |
| Group Delay (Note 32) | | GD | | 5.9 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 80kHz | | FR | -2.00 | | -0.00 | dB |

2-4 Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SLOW ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.05dB | PB | 0 | | 10.1 | kHz |
| | -3.0dB | PB | | 20.24 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 31) | | SB | 43.0 | | | kHz |
| Stopband Attenuation (Note 33) | | SA | 74.9 | | | dB |
| Group Delay (Note 32) | | GD | | 5.2 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 20kHz | | FR | -3.50 | | -2.50 | dB |

fs=96kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SLOW ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.05dB | PB | 0 | | 20.3 | kHz |
| | -3.0dB | PB | | 40.50 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 31) | | SB | 86.0 | | | kHz |
| Stopband Attenuation (Note 33) | | SA | 74.9 | | | dB |
| Group Delay (Note 32) | | GD | | 5.2 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 40kHz | | FR | -4.00 | | -2.50 | dB |

fs=192kHz

| Parameter | | Symbol | min | typ | max | Unit |
|----------------------------------|-----------------|--------|-------|-------|-------|------|
| SHORT DELAY SHARP ROLL-OFF | | | | | | |
| Passband (Note 31) | -0.07dB~+0.05dB | PB | 0 | | 40.6 | kHz |
| | -3.0dB | PB | | 81.00 | | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 31) | | SB | 172.0 | | | kHz |
| Stopband Attenuation (Note 33) | | SA | 74.9 | | | dB |
| Group Delay (Note 32) | | GD | | 5.2 | | 1/fs |
| Digital Filter + SCF | | | | | | |
| Frequency Response : 0Hz ~ 80kHz | | FR | -4.75 | | -2.75 | dB |

Note 31. The passband and stopband frequencies are proportional to fs (sampling rate).

Note 32. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/24/32-bit impulse data to the input registers to output of the analog peak signal.

Note 33. Band width of Stopband Attenuation ranges from SB to fs.

3. SRC Block

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

| Parameter | | Symbol | min | typ | max | Unit | |
|---------------------------------------|---------|---|-----|--------------------------|-----|-----------|-----|
| Passband | -0.01dB | $0.980 \leq \text{FSO/FSI} \leq 6.000$ | PB | 0 | | 0.4583FSI | kHz |
| | -0.01dB | $0.900 \leq \text{FSO/FSI} < 0.990$ | PB | 0 | | 0.4167FSI | kHz |
| | -0.01dB | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 35) | PB | 0 | | 0.2182FSI | kHz |
| | -0.50dB | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 36) | PB | 0 | | 0.3007FSI | kHz |
| | -0.01dB | $0.490 \leq \text{FSO/FSI} < 0.539$ | PB | 0 | | 0.2177FSI | kHz |
| | -0.01dB | $0.450 \leq \text{FSO/FSI} < 0.495$ | PB | 0 | | 0.1948FSI | kHz |
| | -0.01dB | $0.225 \leq \text{FSO/FSI} < 0.455$ | PB | 0 | | 0.1312FSI | kHz |
| | -0.50dB | $0.167 \leq \text{FSO/FSI} < 0.227$ | PB | 0 | | 0.0658FSI | kHz |
| Stopband | | $0.980 \leq \text{FSO/FSI} \leq 6.000$ | SB | 0.5417FSI | | | kHz |
| | | $0.900 \leq \text{FSO/FSI} < 0.990$ | SB | 0.5021FSI | | | kHz |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 35) | SB | 0.2974FSI | | | kHz |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 36) | SB | 0.3320FSI | | | kHz |
| | | $0.490 \leq \text{FSO/FSI} < 0.539$ | SB | 0.2812FSI | | | kHz |
| | | $0.450 \leq \text{FSO/FSI} < 0.495$ | SB | 0.2604FSI | | | kHz |
| | | $0.225 \leq \text{FSO/FSI} < 0.455$ | SB | 0.1802FSI | | | kHz |
| | | $0.167 \leq \text{FSO/FSI} < 0.227$ | SB | 0.0970FSI | | | kHz |
| Passband Ripple | | $0.900 \leq \text{FSO/FSI} \leq 6.000$ | PR | | | ±0.01 | dB |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 35) | PR | | | ±0.01 | dB |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 36) | PR | | | ±0.50 | dB |
| | | $0.225 \leq \text{FSO/FSI} \leq 0.539$ | PR | | | ±0.01 | dB |
| | | $0.167 \leq \text{FSO/FSI} < 0.227$ | PR | | | ±0.50 | dB |
| Stopband Attenuation | | $0.900 \leq \text{FSO/FSI} \leq 6.000$ | SA | 95.2 | | | dB |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 35) | SA | 95.2 | | | dB |
| | | $0.533 \leq \text{FSO/FSI} < 0.909$ (Note 36) | SA | 90.0 | | | dB |
| | | $0.450 \leq \text{FSO/FSI} \leq 0.539$ | SA | 95.2 | | | dB |
| | | $0.225 \leq \text{FSO/FSI} < 0.455$ | SA | 90.0 | | | dB |
| | | $0.167 \leq \text{FSO/FSI} < 0.227$ | SA | 85.0 | | | dB |
| Group Delay (Ts=1/fs) (Note 34) | | GD | | 61 (54/FSI+ 7/FSO) | | | Ts |

Note 34. This value is SRC block only. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

Note 35. In the case of SRCFAUD bit = "1"

Note 36. In the case of SRCFAUD bit = "0"

4. FSCONV

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V;
VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

| Parameter | | | Symbol | min | typ | max | Unit |
|-------------------------------------|---------|--|--------|-----------|-----|-----------|------|
| Passband | -0.01dB | $0.167 \leq \text{FSO/FSI} \leq 0.363$ | PB | 0 | | 0.1814FSI | kHz |
| Stopband | | $0.167 \leq \text{FSO/FSI} \leq 0.363$ | SB | 0.8185FSI | | | kHz |
| Passband Ripple | | $0.167 \leq \text{FSO/FSI} \leq 0.363$ | PR | | | ±0.005 | dB |
| Stopband Attenuation | | $0.167 \leq \text{FSO/FSI} \leq 0.363$ | SA | 94.0 | | | dB |
| Group Delay (Ts=1/FSI) (Note 37) | | | GD | | 9 | | Ts |

Note 37. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

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|-------------------------------|
| 10. DC Characteristics |
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■ DC Characteristics

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD3=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

| Parameter | Symbol | min | typ | max | Unit |
|---|-------------------------|-----------|----------|----------|------|
| High-Level Input Voltage 1 (Note 38) | VIH1 | 80%TVDD1 | | | V |
| Low-Level Input Voltage 1 (Note 38) | VIL1 | | | 20%TVDD1 | V |
| High-Level Input Voltage 2 (Note 39) | VIH2 | 80%TVDD2 | | | V |
| Low-Level Input Voltage 2 (Note 39) | VIL2 | | | 20%TVDD2 | V |
| High-Level Input Voltage 3 (Note 40) | VIH3 | 80%VDD33 | | | V |
| Low-Level Input Voltage 3 (Note 40) | VIL3 | | | 20%VDD33 | V |
| SCL, SDA High-Level Input Voltage | VIH4 | 70%TVDD2 | | | V |
| SCL, SDA Low-Level Input Voltage | VIL4 | | | 30%TVDD2 | V |
| High-Level Output Voltage Iout= -100μA (Note 38) | VOH1 | TVDD1-0.3 | | | V |
| Low-Level Output Voltage Iout=100μA (Note 38) | VOL1 | | | 0.3 | V |
| High-Level Output Voltage Iout= -100μA (Note 39) | VOH2 | TVDD2-0.3 | | | V |
| Low-Level Output Voltage Iout=100μA (Note 39) | VOL2 | | | 0.3 | V |
| High-Level Output Voltage Iout= -100μA (Note 40) | VOH3 | VDD33-0.3 | | | V |
| Low-Level Output Voltage Iout=100μA (Note 40) | VOL3 | | | 0.3 | V |
| SCL, SDA Low Level Output Voltage | Fast Mode | | | | |
| | TVDD2 ≥ 2.0V (Iout=3mA) | VOL4 | | 0.4 | V |
| | TVDD2 < 2.0V (Iout=3mA) | VOL4 | | 20%TVDD2 | V |
| | Fast Mode Plus | | | | |
| TVDD2 ≥ 2.0V (Iout=20mA) | VOL4 | | 0.4 | V | |
| TVDD2 < 2.0V (Iout=3mA) | VOL4 | | 20%TVDD2 | V | |
| Input Leak Current (Note 41) | Iin | | | ±10 | μA |
| Input Leak Current, Pulled down pin Power Down (Note 42) | Iid | | 66 | | μA |
| Input Leak Current, Pulled down pin Power Down Release (Note 43) | Iid | | 72 | | μA |
| Input Leak Current, TESTI pin | lid | | 132 | | μA |
| Input Leak Current, XTI pin | lix | | 17 | | μA |

Note 38. SDIN1, SDIN2/JX0, SDOUT1, SDOUT2/GPO0, LRCK1, BICK1, LRCK2 and BICK2 pins.

Note 39. SDIN3/JX1, SDIN4, SDOUT3/GPO1, STO/RDY/SDOUT4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN, and SI/I2CFIL pins. The SCL and SDA pins are not included.

Note 40. SDIN5/JX0, SDIN6, SDOUT5/GPO2, SDOUT6/DIT/GPO3, LRCK5, BICK5, CLKO, XTO, XTI and TESTI pins

Note 41. Except internal pulled-down pins and the XTI pin.

Note 42. LRCK5, BICK5, LRCK2, BICK2, LRCK1, BICK1, LRCK3/JX2, BICK3/JX3, LRCK4 and BICK4 pins are internal pulled-down pins (typ. 50 kΩ@3.3V) when the AK7738 is powered down (PDN pin = "L"). The TESTI pin is not included.

Note 43. LRCK5, BICK5, LRCK2, BICK2, LRCK1, BICK1, LRCK3/JX2, BICK3/JX3, LRCK4 and BICK4 pins are internal pulled-down pins (typ. 46 kΩ@3.3V) when power-down is released (PDN pin = "H"). The TESTI pin is not included.

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| 11. Switching Characteristics |
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1. System Clock

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V;
VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----------|---------|--------|------|
| XTI Input Timing | | | | | |
| a) X'tal Oscillator | | | | | |
| Input Frequency | fXTI | 11.2896 | | 18.432 | MHz |
| b) XTI Clock Input | | | | | |
| Duty Cycle | | 40 | 50 | 60 | % |
| Input Frequency | fXTI | 0.256 | | 24.576 | MHz |
| CLKO Output Timing | | | | | |
| Output Frequency | fCLKO | 2.048 | | 24.576 | MHz |
| Duty Cycle | dCLKO | | 50 | | % |
| LRCK/BICK Input Timing (Slave Mode) | | | | | |
| LRCK Input Timing | | | | | |
| Frequency | fs | 8 | | 192 | kHz |
| BICK Input Timing | | | | | |
| Frequency (Note 44) | fBCLK | 0.256 | | 24.576 | MHz |
| Pulse Width Low | tBCLKL | 0.4/fBCLK | | | ns |
| Pulse Width High | tBCLKH | 0.4/fBCLK | | | ns |
| LRCK/BICK Output Timing (PLL Master Mode) | | | | | |
| LRCK Output Timing | | | | | |
| Frequency | fs | 8 | | 192 | kHz |
| Pulse Width High | tLRCKH | | 1/fBCLK | | ns |
| PCM Mode | tLRCKH | | 50 | | % |
| Except PCM Mode | tLRCKH | | | | % |
| BICK Output Timing | | | | | |
| Frequency (Note 44) | fBCLK | 0.256 | | 24.576 | MHz |
| Duty | dBCLK | | 50 | | % |

Note 44. Required to meet the following expression: $fBCLK \geq 2 \times fs \times (\text{Input/Output Data Length})$.

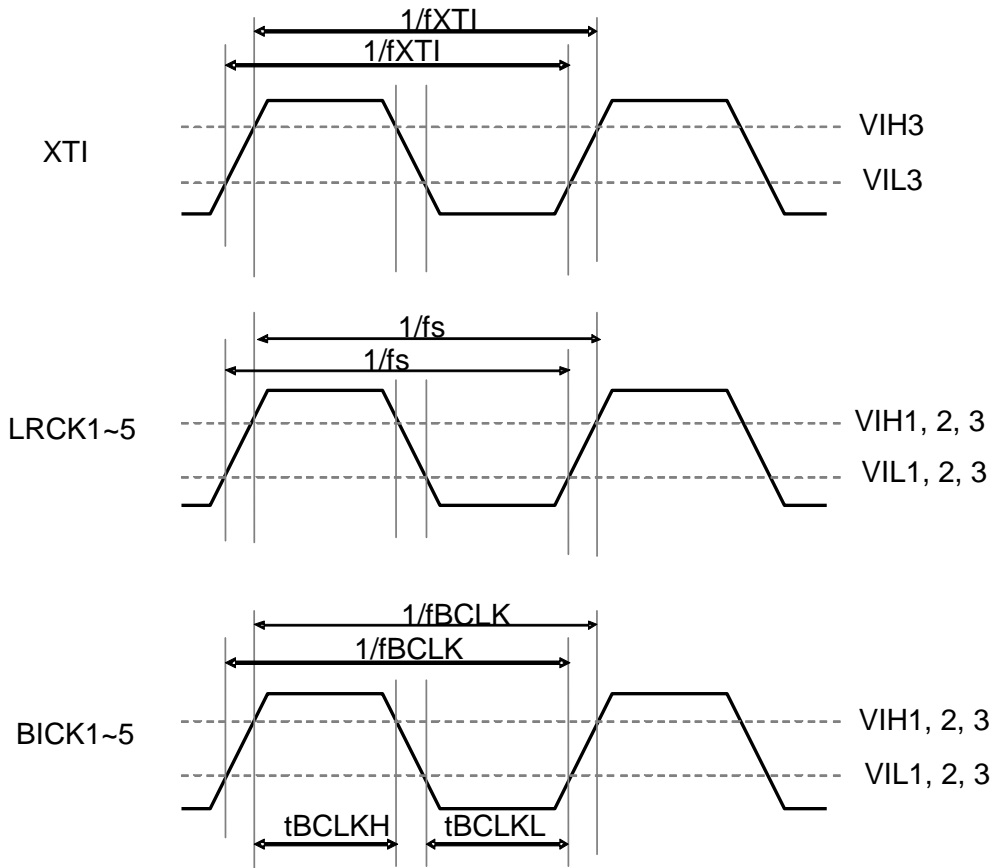


Figure 5. System Clock Timing

2. Power Down

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

| Parameter | Symbol | Min | typ | max | Unit |
|---------------------------|--------|-----|-----|-----|------|
| PDN Pluse Width (Note 45) | tRST | 600 | | | ns |

Note 45. The PDN pin must be “L” when power up the AK7738.

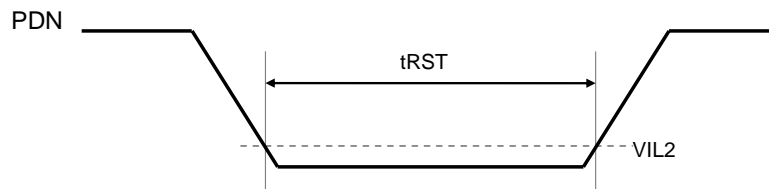


Figure 6. Reset Timing

3. Serial Data Interface (SDIN1 ~ SDIN6, SDOUT1 ~ SDOUT6)

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V;
VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-------------------------|-----|------|
| Slave Mode | | | | | |
| Delay Time from BICK “↑” to LRCK (Note 46) | tBLRD | 10 | | | ns |
| Delay Time from LRCK to BICK “↑” (Note 46) | tLRBD | 10 | | | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 10 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 5 | | | ns |
| Delay Time from BICK “↓” to Serial Data Output (Note 47) | tBSOD1 | | | 20 | ns |
| Delay Time from BICK “↑” to Serial Data Output (Note 46, Note 48) | tBSOD2 | 5 | | 30 | ns |
| Master Mode | | | | | |
| BICK frequency | fBCLK | - | 32, 48, 64, 128, 256 | - | fs |
| BICK Duty cycle | | | 50 | | % |
| Delay Time from BICK “↓” to LRCK (Note 47) | tMBL | -10 | | 10 | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 20 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 10 | | | ns |
| Delay Time from BICK “↓” to Serial Data Output (Note 47, Note 48) | tBSOD | | | 10 | ns |

Note 46. It is measured from BICK “↓” when the BICK polarity is inverted by setting BCKPx bit = “1”.

Note 47. It is measured from BICK “↑” when the BICK polarity is inverted by setting BCKPx bit = “1”.

Note 48. Set SDOPHx bit to “1” and the data should be output based on BICK “↑” when using TDM256 mode with 96kHz sampling frequency in slave mode. SDOPHx bit must be set to “0” in master mode.

3-1. Slave Mode

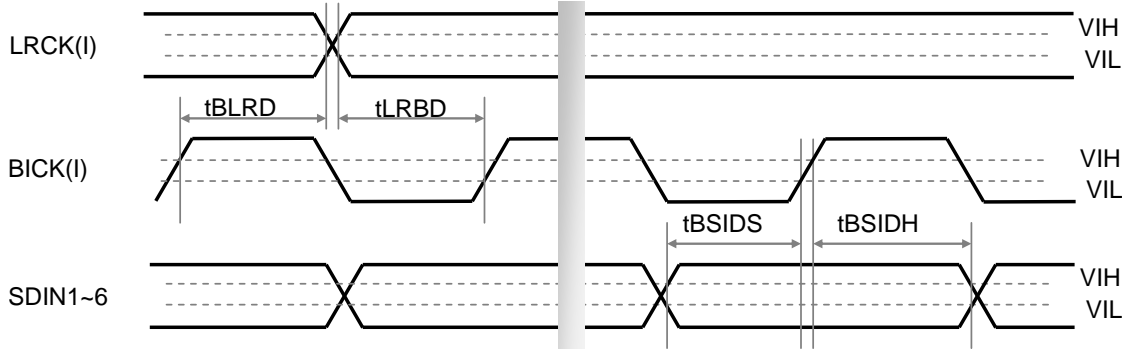


Figure 7. Serial Interface Input Timing in Slave Mode

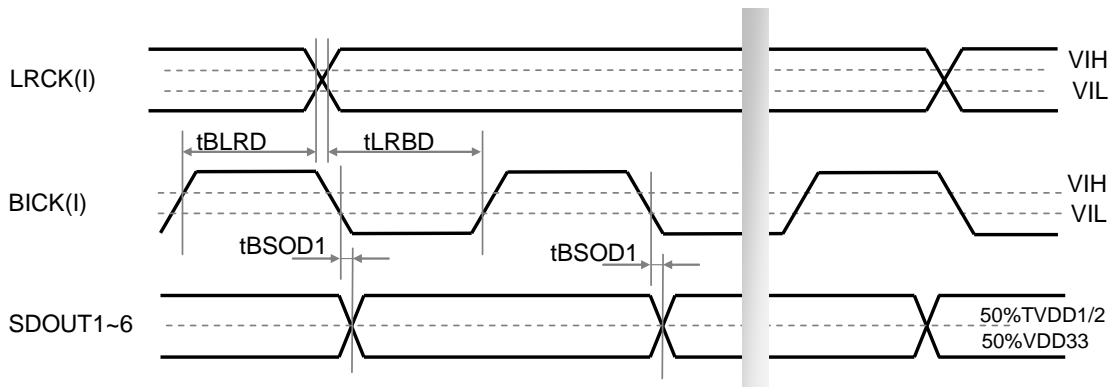


Figure 8. Serial Interface Output Timing in Slave Mode (SDOPHx bit = "0")

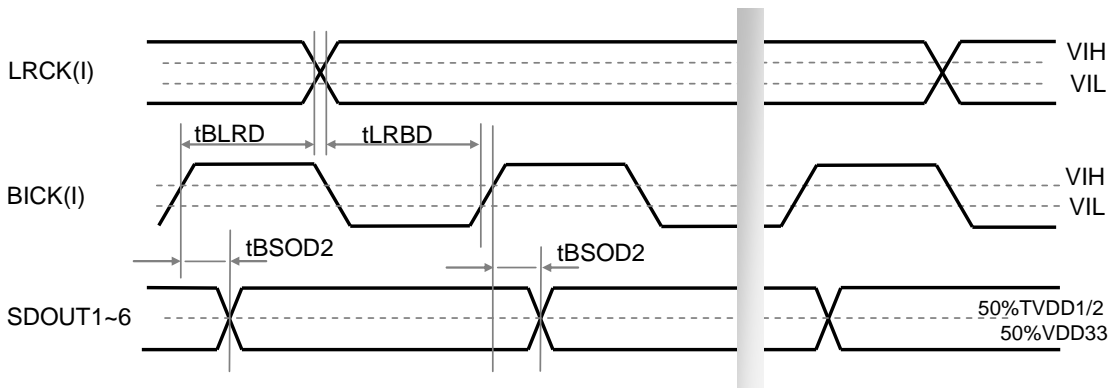


Figure 9. Serial Interface Output Timing in Slave Mode (SDOPHx bit = "1")

3-2. Master Mode

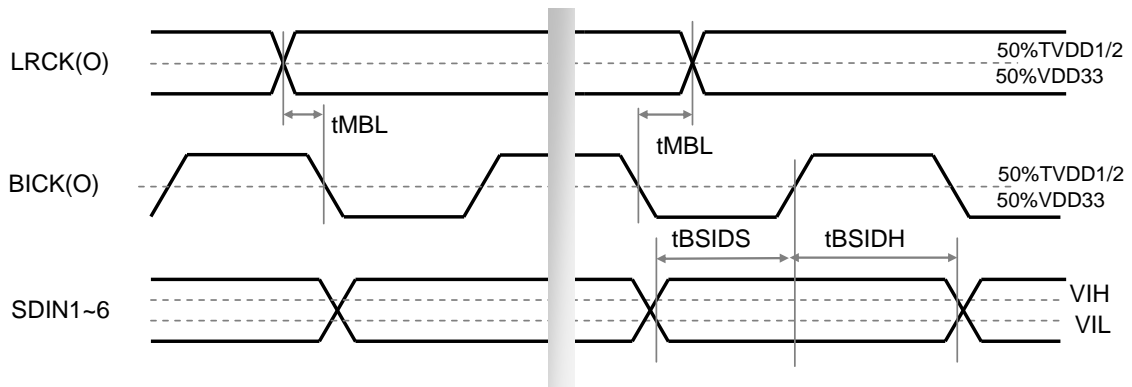


Figure 10. Serial Interface Input Timing in Master Mode

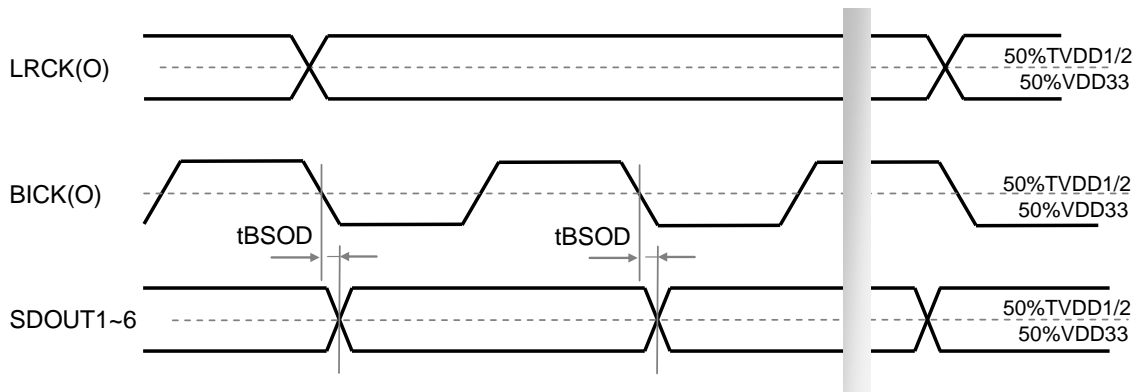


Figure 11. Serial Interface Output Timing in Master Mode (SDOPHx bit = "0")

4. SPI Interface

4-1. Clock Reset (CKRESETN bit = "0")

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| μP Interface Signal | | | | | |
| SCLK Frequency (Note 51) | fSCLK | | | 3.5 | MHz |
| SCLK Low-level Width | tSCLKL | 120 | | | ns |
| SCLK High-level Width | tSCLKH | 120 | | | ns |
| Microcontroller → AK7738 | | | | | |
| CSN High-level Width | tWRQH | 300 | | | ns |
| From CSN "↑" to PDN "↑" | tRST | 360 | | | ns |
| From PDN "↑" to CSN "↓" | tIRRQ | 1 | | | ms |
| From CSN "↓" to SCLK "↓" | tWSC | 300 | | | ns |
| From SCLK "↑" to CSN "↑" | tSCW | 480 | | | ns |
| SI Latch Setup Time | tSIS | 120 | | | ns |
| SI Latch Hold Time | tSIH | 120 | | | ns |
| AK7738 → Microcontroller | | | | | |
| Delay Time from SCLK "↓" to SO Output | tSOS | | | 120 | ns |
| SO Output Hold Time from SCLK "↑" (Note 49) | tSOH | 120 | | | ns |

Note 49. Except when writing the 24th bit (8 bits command + 16 bits address) of the command code. This will be the 8th bit (8 bits command) with "write preparation data read command (24H and 25H)".

4-2. PLL Lock (CKRESETN bit = "1" and PLL is locked)

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| μP Interface Timing (SPI mode) | | | | | |
| SCLK Frequency (Note 50) (Note 51) | fSCLK | | | 7 | MHz |
| SCLK Low Level Width | tSCLKL | 60 | | | ns |
| SCLK High Level Width | tSCLKH | 60 | | | ns |
| μP → AK7738 | | | | | |
| CSN High Level Width | tWRQH | 150 | | | ns |
| From CSN "↑" to PDN "↑" | tRST | 180 | | | ns |
| From PDN "↑" to CSN "↓" | tIRRQ | 1 | | | ms |
| From CSN "↓" to SCLK "↓" | tWSC | 150 | | | ns |
| From SCLK "↑" to CSN "↑" | tSCW | 240 | | | ns |
| SI Latch Setup Time | tSIS | 60 | | | ns |
| SI Latch Hold Time | tSIH | 60 | | | ns |
| AK7738 → μP | | | | | |
| Delay Time from SCLK "↓" to SO Output | tSOS | | | 60 | ns |
| SO Output Hold Time from SCLK "↑" (Note 49) | tSOH | 60 | | | ns |

Note 50. It takes maximum 10ms to lock PLL after setting CKRESETN bit = "0" → "1".

Note 51. Control registers can always be accessed by a maximum speed of 7MHz. Interfacing with the AK7738 except control registers should be made at a maximum speed of 3.5MHz when PLL is unlocked or at a maximum speed of 7MHz when PLL is locked. It is necessary to set DLRDY bit to "1" when interfacing with the AK7738 except control registers if PLL is unlocked.

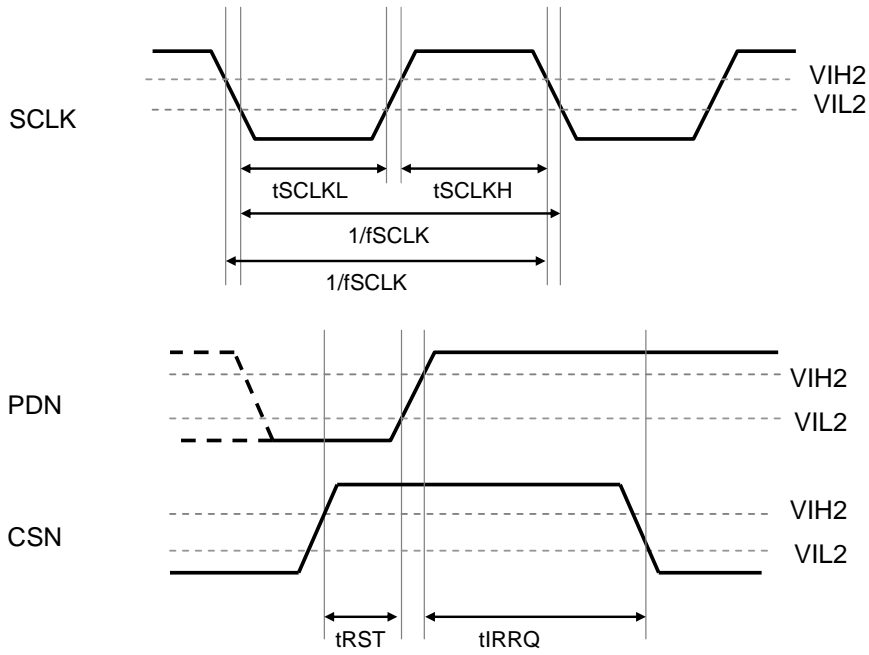


Figure 12. SPI Interface Timing 1

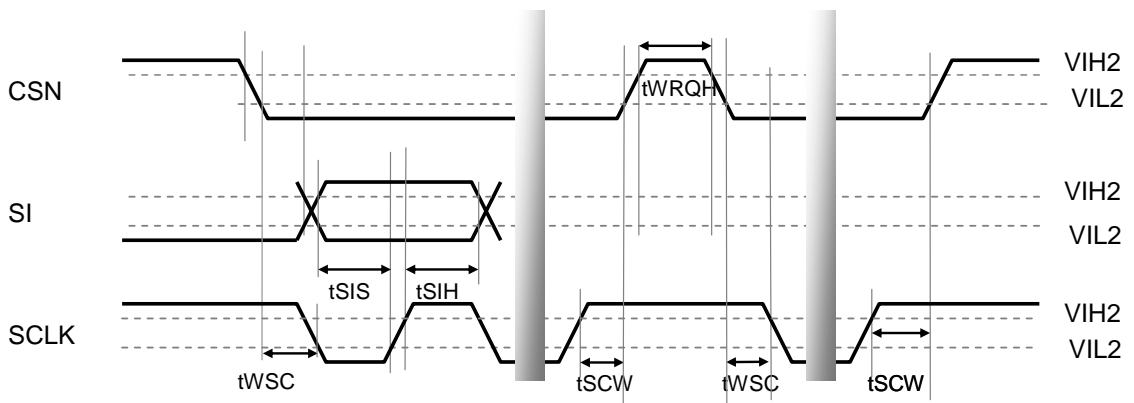


Figure 13. SPI Interface Timing 2 (Microcontroller → AK7738)

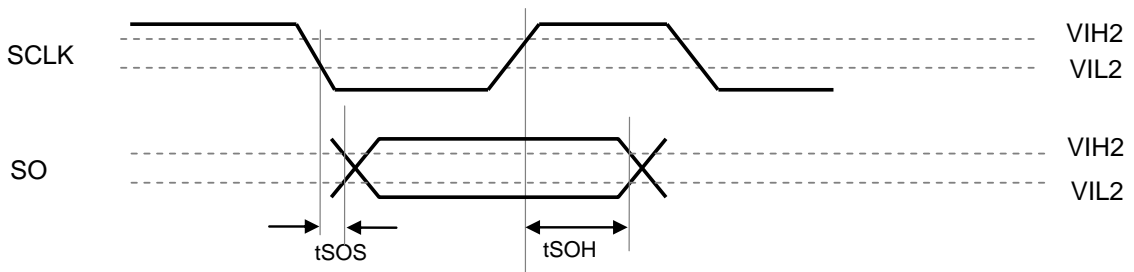


Figure 14. SPI Interface Timing 3 (AK7738 → Microcontroller)

5. I²C Interface

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

<I²C: Fast Mode>

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|-----|-----|-----|------|
| I ² C Timing | | | | | |
| SCL clock frequency | fSCL | - | - | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | - | - | μs |
| Clock Low Time | tLOW | 1.3 | - | - | μs |
| Clock High Time | tHIGH | 0.6 | - | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | - | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | - | - | μs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | - | 50 | ns |
| Capacitive load on bus | Cb | - | - | 400 | pF |

<I²C: Fast Mode Plus>

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|------|-----|------|------|
| I ² C Timing | | | | | |
| SCL clock frequency | fSCL | - | - | 1 | MHz |
| Bus Free Time Between Transmissions | tBUF | 0.5 | - | - | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.26 | - | - | μs |
| Clock Low Time | tLOW | 0.5 | - | - | μs |
| Clock High Time | tHIGH | 0.26 | - | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.26 | - | - | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | - | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.05 | - | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.12 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.12 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.26 | - | - | μs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | - | 50 | ns |
| Capacitive load on bus | Cb | - | - | 550 | pF |

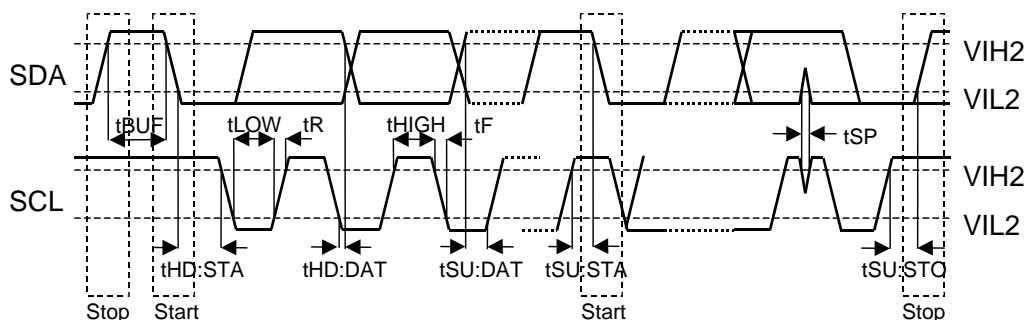
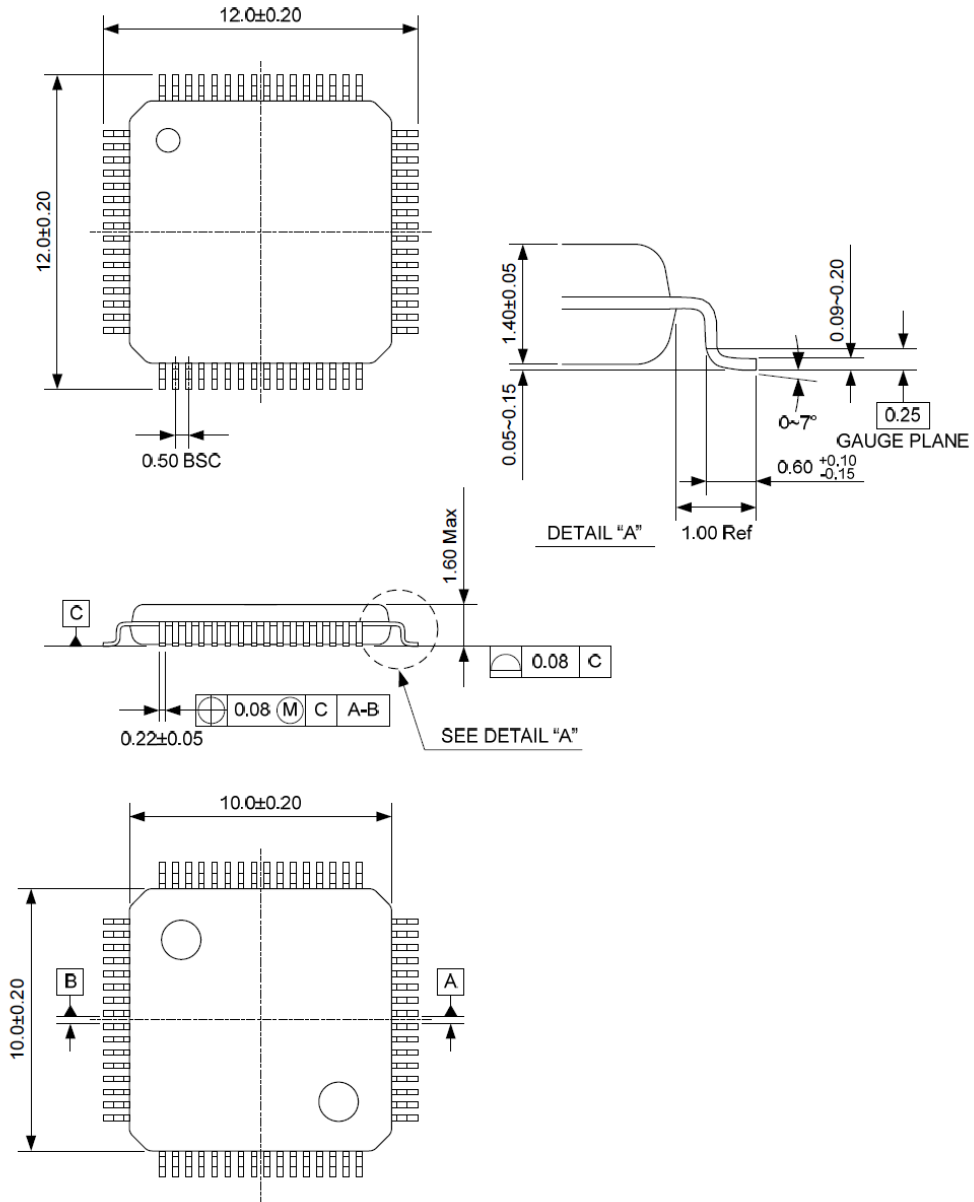


Figure 15. I²C-bus Interface Timing

12. Package

■ **Outline Dimensions**

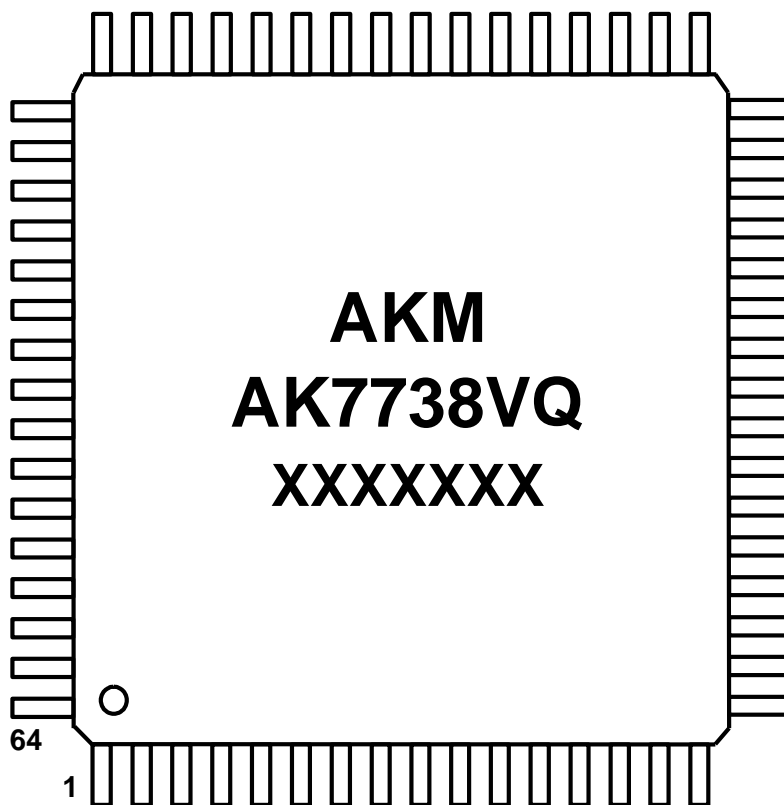
64-pin LQFP (Unit: mm)



■ **Material and Lead Finish**

- Package: Epoxy
- Lead frame: Copper
- Lead-finish: Soldering (Pb free) plate

■ **Marking**



- 1) Pin #1 indication
- 2) Date Code: XXXXXXXX(7 digits)
- 3) Marking Code: AK7738VQ
- 4) Asahi Kasei Logo

13. Revision History

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|--------------|----------|---------------|------|----------|
| 15/01/08 | 00 | First Edition | | |

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